AMENDMENTS TO THE CLAIMS

Please cancel claims 63-156 and add new claims 157-160, all without prejudice.

Listing of Claims

(Claims 1-156 have been cancelled.)

157.(New) A method of operating a non-volatile memory device having a plurality of multi-state memory cells, the multi-states including first, second, third and fourth states having conductivity values decreasing in order of the first state, the second state, the third state and the fourth state, the method including:

writing one or more selected ones of the memory cells to a respective target data value from the multi-states by a process including a series of alternating program and verify operations until the memory cells selected for writing verify at their respective target data values using sense circuitry to verify for each of target state against a corresponding verify reference level, wherein a first, a second, a third and a fourth verify reference level respectively correspond to the first, second, third and fourth of the multi-states,

reading the one or more selected memory cells using the sense circuitry to perform in parallel comparisons with a first read reference level for distinguishing between the first and second states, a second read reference level for distinguishing between the second and third states, and a third read reference level for distinguishing between the third and fourth states,

wherein the first read reference level is allocated between the first and second verify reference levels, the second read reference level is allocated between the second and third verify reference levels, and the third read reference level is allocated between the third and the fourth verify reference levels.

158.(New) The method of claim 157, wherein the memory cells are arranged into an array of rows formed along word lines and columns formed along bit lines, the array having formed along a first side row select circuitry connectable to the word lines and having formed along a second side column select circuitry and the sense circuitry.

159.(New) A non-volatile memory device, including:

an array of non-volatile memory cells formed along rows connected to word lines and columns connected along bit lines, each of the memory cells capable of storing a plurality of data states each corresponding to a distinct threshold voltage range and including, in order of increasing threshold values, a first, a second, a third and a fourth data state;

write circuitry connectable to the memory array to selectively program the individual memory cells to a corresponding target one of the data states; and

read circuitry connectable to the memory array to selectively compare information indicating data stored the individual memory cells to a plurality of reference values, the reference values including: first, second, third and fourth verify values used in a verify operation during the writing of a memory cell to the first, second, third and fourth data state, respectively; and a first read value used to distinguish between the first and second data states in a read operation, a second read value used to distinguish between the second and third data states in a read operation, and a third read value used to distinguish between the third and fourth data states in a read operation,

wherein the first read reference level is allocated between the first and second verify reference levels, the second read reference level is allocated between the second and third verify reference levels, and the third read reference level is allocated between the third and the fourth verify reference levels.

160.(New) A non-volatile memory device, including:

an array of non-volatile memory cells formed along rows connected to word lines and columns connected along bit lines, each of the memory cells capable of storing a plurality of data states each corresponding to a distinct threshold voltage range and including, in order of increasing threshold values, a first, a second, a third and a fourth data state;

sense circuitry connectable to the memory array to selectively compare information indicating data stored the individual memory cells to a plurality of reference values; and

parameter generation circuitry connectable to provide the plurality of reference values to the sense circuitry, the reference values including: first, second, third and fourth verify values used in a verify operation during the writing of a memory cell to the first, second, third and fourth data state, respectively; and a first read value used to distinguish between the first and second data states in a read operation, a second read value used to distinguish between the

second and third data states in a read operation, and a third read value used to distinguish between the third and fourth data states in a read operation,

wherein the first read reference level is allocated between the first and second verify reference levels, the second read reference level is allocated between the second and third verify reference levels, and the third read reference level is allocated between the third and the fourth verify reference levels.